ABSTRACT

According to embodiments of the invention, there is disclosed a computer processor architecture; and in particular a computer processor, a method of operating the same, and a computer program product that makes use of an instruction set for the computer. In one embodiment according to the invention, there is provided a computer processor comprising: a decode unit for decoding a stream of instruction packets from a memory, each instruction packet comprising a plurality of instructions; a first processing channel comprising a plurality of functional units and operable to perform control processing operations; a second processing channel comprising a plurality of functional units and operable to perform data processing operations; wherein the decode unit is operable to receive an instruction packet and to detect if the instruction packet defines (i) a plurality of control instructions or (ii) a plurality of instructions one or more of which is a data processing instruction, and wherein when the decode unit detects that the instruction packet comprises a plurality of control instructions said control instructions are supplied to the first processing channel for execution in program order.